What is Claimed is:

[c1] A diode formed in a substrate having isolation regions, comprising an anode of a first conductivity type and a cathode of a second conductivity type disposed below said anode and in electrical contact with said substrate, wherein at least one of said cathode and anode comprise a plurality of vertically abutting diffusion regions, and wherein said cathode and anode are disposed between adjacent isolation regions that extend deeper into the substrate than said anode and said cathode.

[c2] The diode as recited in claim 1, wherein said isolation regions comprise a plurality of insulation-filled trenches having sidewalls that are substantially vertical.

[c3] The diode as recited in claim 1, wherein said isolation regions comprise a plurality of insulation-filled trenches having sidewalls that are tapered.

[c4] The diode as recited in claim 1, wherein said cathode including a first doped region of a second conductivity type abutting said anode and a second doped region of said second conductivity type abutting and disposed below said first doped region and contacting said substrate, said first and second doped regions having different dopant concentrations.

[c5] The diode as recited in claim 1, further comprising a second pair of isolation structures disposed between said ajacent isolation regions and said anode.

[c6] The diode as recited in claim 1, wherein said anode and said cathode form a pn junction bounded by said isolation regions.

[c7] The diode as recited in claim 1, wherein said isolation regions comprise a plurality of insulating trenches having a depth not greater than approximately 5.5 microns.

[c8] The diode as recited in claim 7, wherein said plurality of insulating trenches are lined with a first material that does not produce dislocations in said substrate.

[c9] The diode as recited in claim 8, wherein said liner comprises silicon oxide.

[c10] The diode as recited in claim 8, wherein said plurality of insulating trenches are filled with a second material having a thermal expansion coefficient that does not damage said substrate.

[c11] The diode as recited in claim 10, wherein said second material is selected from the group consisting of polysilicon, PSG, and BPSG.

[c12] The diode as recited in claim 8, wherein said liner has a thickness of at least 100 Angstroms.

[c13] The diode as recited in claim 6, wherein said cathode forms a pn junction with said substrate that is bounded by said plurality of insulation-filled trenches.

[c14] The diode as recited in claim 4, wherein said cathode further comprises a third doped region disposed between said first doped region and said second doped region.

[c15] The diode as recited in claim 14, wherein said third doped region comprises a retrograde-doped region.

[c16] The diode as recited in claim 3, wherein said anode comprises a first doped region abutting said cathode and a second doped region on a surface of said substrate, said second doped region having a higher concentration of dopant than said first doped region.

[c17] The diode as recited in claim 16, wherein said first doped region comprises a retrograde-doped region.

[c18] The diode as recited in claim 3, further comprising a plurality of diffusion regions of said second conductivity type formed on a surface of said substrate.

[c19] The diode as recited in claim 18, wherein said plurality of diffusion regions are separated from said cathode by respective isolation regions.

[c20] A diode formed in a substrate having isolation regions, comprising an anode of a first conductivity type and a cathode of a second conductivity type disposed below said anode and in electrical contact with said substrate, wherein at least one of said cathode and anode comprise a plurality of vertically abutting diffusion regions, and wherein said cathode and anode are disposed between adjacent trench isolation regions that extend below a junction formed between a lower portion of said cathode and the substrate, and further comprising a second pair of isolation structures disposed between said ajacent isolation regions and said anode.

[c21] The diode as recited in claim 20, wherein said trench isolation regions have sidewalls that are substantially vertical.

[c22] The diode as recited in claim 20, wherein said trench isolation regions have sidewalls that are tapered.

[c23] The diode as recited in claim 21, wherein said cathode includes a first doped region of a second conductivity type abutting said anode and a second doped region of said second conductivity type abutting and disposed below said first doped region and contacting said substrate, said first and second doped regions having different dopant concentrations.

[c24] The diode as recited in claim 23, wherein said anode comprises a first doped region abutting said cathode and a second doped region on a surface of said substrate, said second doped region having a higher concentration of dopant than said first doped region.

[c25] A diode formed on a semiconductor substrate having transistors formed therein with switching speeds in excess of 1GHz, said diode having a capacitance below 0.1pF and a breakdown voltage of at least 500V.

[c26] A method of forming a diode, comprising the steps of:forming an anode of a first conductivity type and a cathode of a second conductivity type disposed below said anode on a substrate, wherein at least one of said cathode and anode comprise a plurality of vertically abutting diffusion regions; and forming a plurality of isolation regions, said cathode and anode being disposed between adjacent ones of said plurality of isolation regions,said plurality of isolation regions extending deeper into said substrate that said cathode and said anode.

[c27] The method as recited in claim 26, wherein said isolation regions comprise a plurality of insulation-filled trenches having sidewalls that are substantially vertical.

[c28] The method as recited in claim 26, wherein said isolation regions comprise a plurality of insulation-filled trenches having sidewalls that are tapered.

[c29] The method as recited in claim 26, wherein said step of forming said cathode comprises: forming a first doped region of a second conductivity type abutting said anode; and forming a second doped region of said second conductivity type abutting and disposed

below said first doped region and contacting said substrate, said first and second doped regions having different dopant concentrations.

[c30] The method as recited in claim 29, further comprising the step of:
forming a second pair of isolation structures disposed between said ajacent isolation regions and said anode.

[c31] The method as recited in claim 26, wherein said isolation regions are formed by a process comprising the steps of:
etching said substrate to form trenches;
depositing at least one insulator; and
removing portions of said insulator outside of said trenches.

[c32] The method as recited in claim 31, wherein said step of depositing comprises a first formation of a liner and a deposition a fill material.

[c33] The method as recited in claim 26, wherein said step of forming said cathode further comprises the step of forming a third doped region disposed between said first doped region and said second doped region.

[c34] The method as recited in claim 33, wherein said third doped region comprises a retrograde-doped region.

[c35] The method as recited in claim 26, wherein said step of forming said anode comprises the steps of:
forming a first doped region abutting said cathode; and
forming a second doped region on a surface of said substrate, said second doped region having a higher concentration of dopant than said first doped region.

[c36] The method as recited in claim 35, wherein said first doped region comprises a retrograde-doped region.

[c37] The method as recited in claim 35, further comprising the steps of:
forming a plurality of diffusion regions of said second conductivity type on a surface of said substrate.

[c38] The method as recited in claim 37, further comprising the step of:

forming a plurality of second isoltion regions that separate said plurality of diffusion regions from said cathode.